

Fig. 1
(Prior Art)

Fig. 2

FIG. 2 is a block diagram of a system for processing video data. The system includes a Graphics Controller (208) and an HDTV Encoder (224). The Graphics Controller (208) provides a Clock signal (212) to the HDTV Encoder (224). The HDTV Encoder (224) receives Input Data (210) and provides a Clock signal (216) to the Graphics Controller (208). The HDTV Encoder (224) also provides a VSYNC Signal (264) and an HSYNC Signal (262) to the Graphics Controller (208). The HDTV Encoder (224) includes four DACs (246, 248, 250, 252) which provide signals (254, 256, 258, 260) to an HDTV Monitor (298). The HDTV Monitor (298) displays the video data.

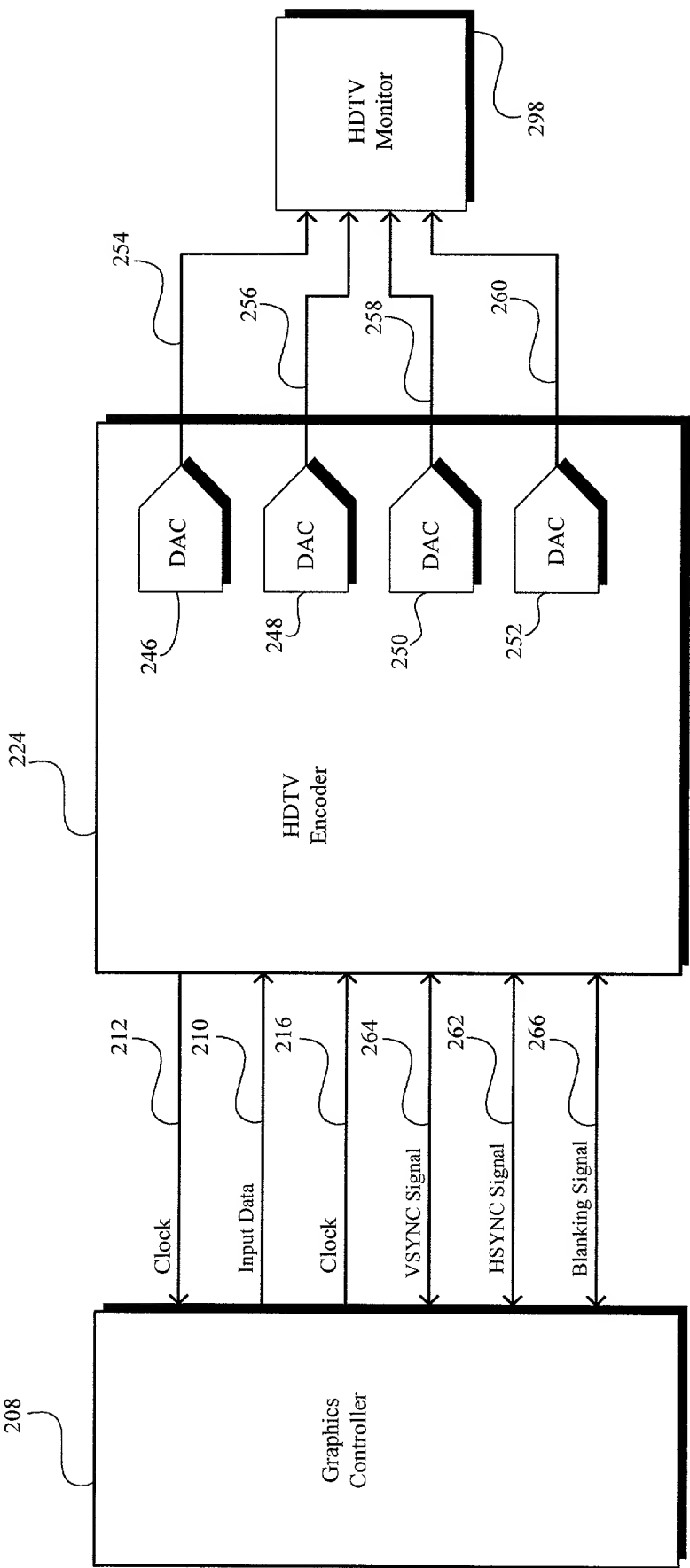
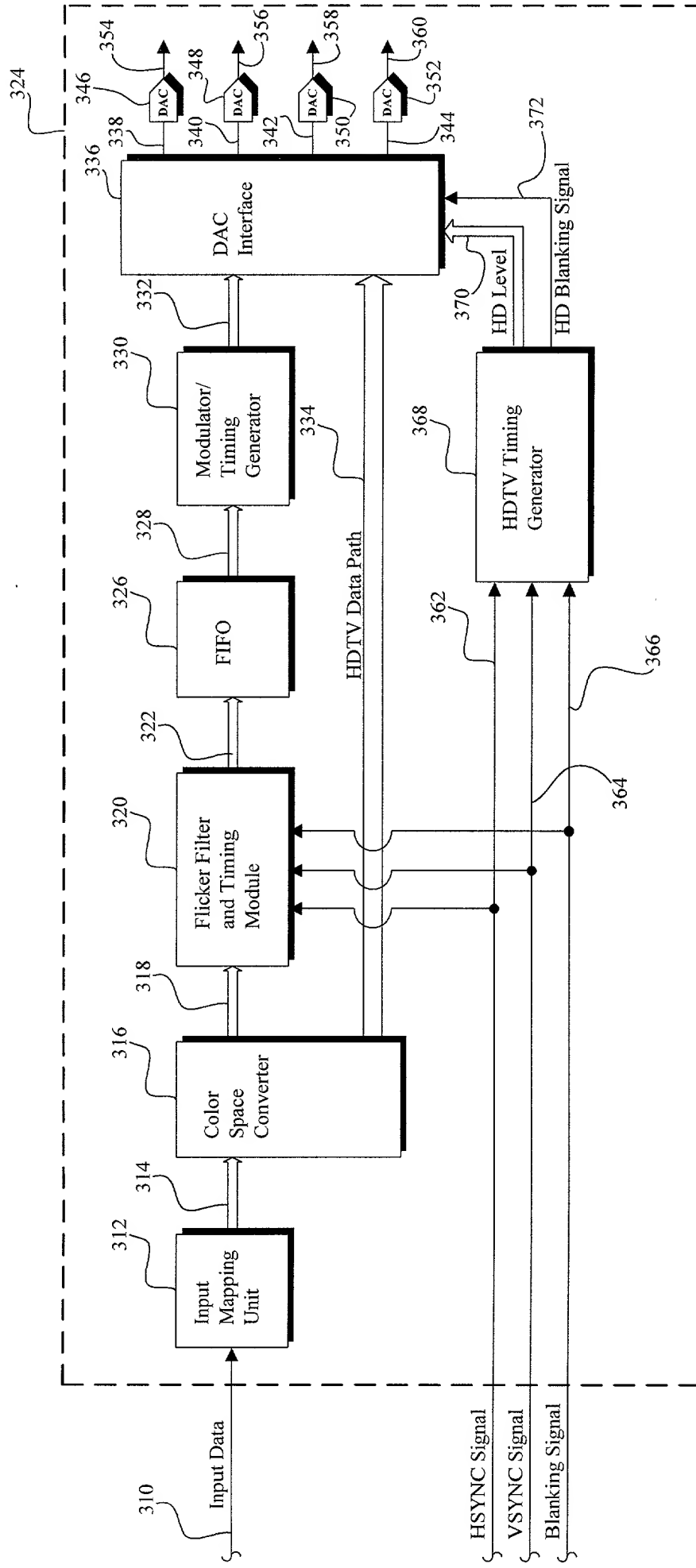


Fig. 3



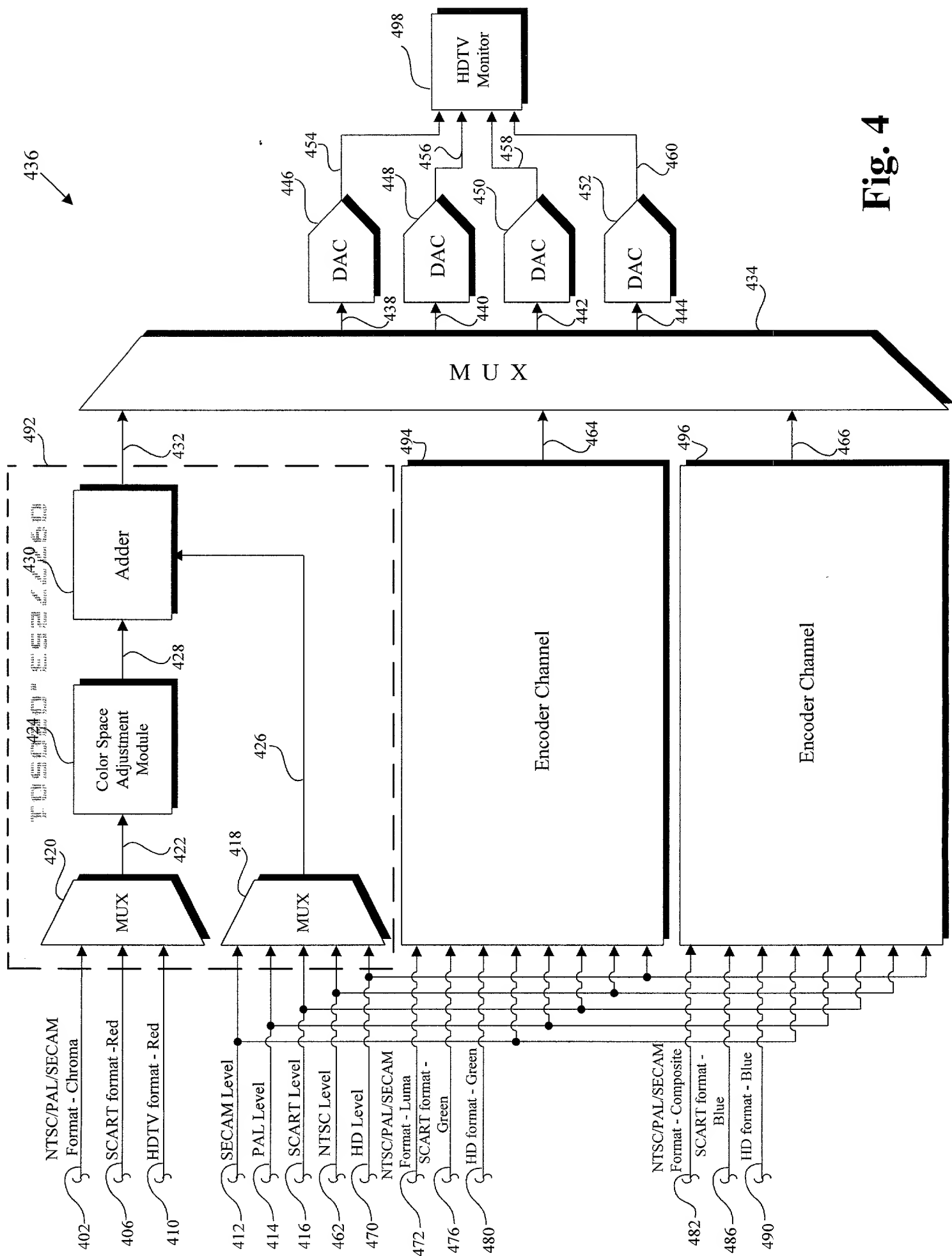


Fig. 4

Fig. 5

